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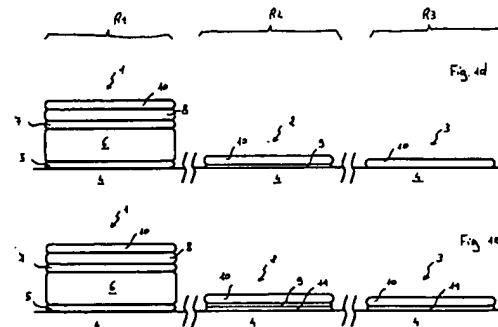
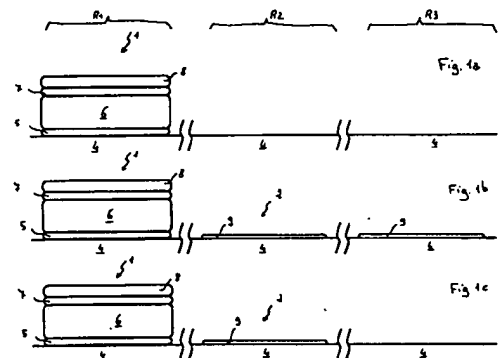
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(54) Process for forming an integrated circuit comprising non-volatile memory cells and side transistors of at least two different types, and corresponding IC

(57) A process for forming an integrated circuit calls for the provision of at least one matrix of non-volatile memory cells (1) including an intermediate dielectric multilayer comprising a lower silicon oxide layer (7), an intermediate silicon nitride layer (8) and an upper silicon oxide layer (10) and the simultaneous provision in zones peripheral to the memory cells of at least one first (2) and one second (3) transistor type having gate dielectric of a first and a second thickness respectively. After formation of the floating gate of the cells with a gate oxide layer (5) and a polycrystalline silicon layer (6) and the formation of the lower silicon oxide layer (7) and of the intermediate silicon nitride layer (8), the process in accordance with the present invention includes:

- removal of said layers from the zones peripheral (R2,R3) to the matrix;
- formation of a first silicon oxide layer (9) over the substrate in the areas (R2,R3) of both types of transistor (2,3);
- removal of the preceding layer (9) from areas (R3) assigned only to the transistors (3) of the second type;
- deposition of said upper silicon oxide layer (10) over the memory cells (1), over the first silicon oxide layer (9) in the areas (R2) of the transistors (2) of the first type and over the substrate (4) in the areas (R3) of the transistors of the second type; and
- formation of a second silicon oxide layer (11) in the

areas (R2,R3) of both types of peripheral transistors (2,3).



EP 0 751 560 A1

Description

Field of application

The present invention relates to a process for forming an integrated circuit comprising non-volatile memory cells and peripheral transistors of at least two different types.

Specifically the present invention relates to a process providing for the implementation in a monocrystalline silicon substrate of at least one matrix of memory cells in each of which a floating gate and a control gate, both electroconductive, are mutually electrically insulated by means of an intermediate dielectric multilayer. There is also provided simultaneous formation in zones peripheral to the matrix of at least one first and one second MOS transistor types.

The present invention also relates to an integrated circuit of the above mentioned type comprising non-volatile memory cells having an intermediate dielectric multilayer and at least two types of peripheral transistors.

Prior art

As well known, in the field of electronic semiconductor technology, to reduce the area of integrated circuits there is a tendency towards ever greater integration scales with a reduction of component sizes. This has led to improvement of the quality of the materials used and to optimization of the processes for their formation.

The present invention falls in particular in the field of the development of the techniques of formation of dielectric materials which in a single integrated circuit and in the form of layers of different thickness and composition perform different functions. On the one hand they act as insulators providing electrical insulation of conductive layers and creating a barrier against contaminating substances coming from the outside environment and on the other hand as active dielectrics allowing the passage of charges between layers of conductive materials.

In order to improve the quality and functionality of the above mentioned dielectrics it has been proposed in relatively recent times to provide multiple superimposed layers, in particular of silicon oxides and/or silicon nitrides.

In the specific field of application of the present invention there are provided integrated memory circuits including, in addition to a plurality of memory cells arranged in one or more matrixes, external or peripheral circuits in which components are structurally similar to the cells and are provided by the same technology. Specific reference is made to MOS transistors.

Non-volatile memories, to which specific reference will be made in the present invention, comprise different classes of devices or products which differ from each other by the structure of the individual memory cell and

the type of application. Specifically reference is made to read-only memories which can be electrically programmed and erased (Erasable Programmable Read Only Memories) and specifically EPROM, EEPROM or FLASH. These can be distinguished as some of them are both erasable and electrically programmable while others require e.g. ultraviolet light to be erased. For data storage, memory cells comprise in all cases a floating-gate MOS transistor integrated on a substrate usually of monocrystalline silicon. The amount of charge contained in the floating gate determines the logical state of the cell. Non-volatile memory cells are programmed in a discrete number of logical states allowing memorization of one or more bits per cell. In standard cells for example programming is provided in two logical states, written and erased, with memorization of one bit per cell.

The floating gate of electroconductive material, normally polysilicon, i.e. polycrystalline silicon or more briefly 'poly', is completely surrounded by insulating material. In particular over the floating gate a dielectric layer, so-called intermediate dielectric or interpoly, insulates the floating gate from an overlying control gate also of electroconductive material. The control gate can consist alternatively of a single polysilicon layer or of a double polysilicon-silicide layer and is coupled electrically to a programming terminal.

As known to those skilled in the art interpoly dielectric is particularly critical as concerns charge retention. Development of the technology has indicated as particularly advantageous the use of a multilayer intermediate dielectric. This preserves the insulating characteristics of the intermediate layer while avoiding the problem of loss of charge by the floating gate to the control gate, whether in the long term or when a high programming potential is applied to the control gate. In particular, as known to those skilled in the art, this class of intermediate dielectrics comprises a triple layer of silicon oxide, silicon nitride and silicon oxide, the so-called ONO. As described e.g. in Patent US-5,104,819, advantageously after formation of an underlying silicon oxide layer and deposition of silicon nitride, an upper silicon oxide layer is formed by deposition instead of by the conventional oxidation of the underlying nitride. The dielectric achieved has good charge retention capability and increased capacitive coupling between floating gate and control gate.

As concerns the so-called external or peripheral transistors, they are incorporated in circuits outside the memory cell matrix, e.g. logical, or matrix control circuits. Specifically in the framework of the present invention reference is made, as indicated above, to MOS transistors.

These transistors include an active dielectric, the so-called gate dielectric, placed between the substrate and a gate of electroconductive material, normally polysilicon. The thickness of this dielectric characterizes the transistor type in terms of electrical properties. In the same circuit are sometimes integrated two types of transistors of the external circuitry having gate dielectric of

different thickness. Usually the active dielectric consists of a silicon oxide layer formed at high temperature by oxidation of the substrate.

To minimize the number of production process steps of the entire integrated circuit it is known that the memory cells and peripheral transistors are made simultaneously, as mentioned above. Specifically the present invention falls within a class of processes in which the polysilicon layer making up the gate of the transistors corresponds in the formation process step to the control gate polysilicon layer of the memory cells. In these processes furthermore the intermediate dielectric of the memory cells and the gate dielectric of the transistors of the circuitry are formed simultaneously.

A known process, in which it is necessary to form two types of peripheral transistors with differentiated gate oxide thickness, comprises essentially the following steps:

- formation in succession of a gate silicon oxide layer of the cells, of a first polysilicon layer of the floating gate and of the intermediate dielectric;
- removal of the above mentioned layers from the zones in which are formed the transistors of the circuitry;
- formation, by means of high-temperature substrate oxidation, of a silicon oxide layer in the areas in which are to be formed the peripheral transistors;
- removal of the silicon oxide layer from the areas of the second transistor type;
- formation, again by substrate oxidation, of another silicon oxide layer in the areas of both types of transistor; and
- formation of a second polysilicon layer of the control gate of the cells and which also constitutes the gate of the peripheral transistors.

Recently in the framework of the research for new types of dielectrics as concerns MOS transistors there was proposed use of a gate dielectric comprising, in addition to a silicon oxide layer achieved by high-temperature thermal oxidation, an overlying layer also of silicon oxide achieved however by deposition. The benefits of such a composite dielectric are described for example in an article entitled "Thin CVD stacked gate dielectric for ULSI technology" by Hsing-Huang Tseng et al, IEDM Technical Digest, page 321-324, 1993.

In patent US-5,104,819 above mentioned there is indicated formation of a memory cell matrix having ONO type interpoly dielectric and peripheral transistors with gate dielectric including another deposited silicon oxide layer. The deposited silicon oxide layer of the intermediate dielectric multilayer of the cells also constitutes the gate dielectric upper layer of the peripheral

transistors and is formed successively over a first gate thermal silicon oxide layer.

This manufacturing process however only permits formation of a single type of peripheral transistor. In addition the silicon oxide deposited to complete the gate dielectric is not good quality if its deposition is not followed by a so-called thermodynamic annealing process, as indicated to be necessary also in the above mentioned article.

The technical problem underlying the present invention is to conceive a process for the formation of non-volatile memory cells and peripheral transistors permitting achievement of a gate dielectric and an intermediate dielectric of good quality, to achieve an integrated circuit having characteristics of great reliability and functionality. This circuit should be provided while minimizing the number of process steps and thus the production costs.

The process which is the purpose of the present invention should also be particularly flexible and usable for example for the simultaneous formation of peripheral transistors having differentiated gate dielectrics.

Summary of the invention

In accordance with the present invention a process for the formation of an integrated circuit in a monocrystalline silicon substrate calls for the provision of at least one matrix of non-volatile memory cells in each of which a floating gate and a control gate, both electroconductive, are electrically insulated from each other by means of an intermediate dielectric multilayer comprising a lower silicon oxide layer, an intermediate silicon nitride layer and an upper silicon oxide layer. The process also comprises simultaneous realization in peripheral zones of the matrix of at least a first and a second transistors types having gate dielectric of a first and a second thickness respectively. There is considered in particular a process of the type in which the gate dielectric of the transistors is formed concomitantly with the intermediate dielectric multilayer of the memory cells.

In accordance with the present invention, after formation of the floating gate with a gate oxide layer and a polycrystalline silicon layer as well as formation of the lower silicon oxide layer and of the intermediate silicon nitride layer, formation of the intermediate dielectric multilayer and of the gate dielectric calls for the following process steps:

- removal from the zones peripheral to the matrix of the above mentioned layers;
- formation of a first silicon oxide layer over the substrate in the areas of both types of transistors;
- removal of the previous layer from the areas assigned only to the transistors of the second type;
- deposition of said upper silicon oxide layer over the

memory cells, over the first silicon oxide layer in the areas of the transistors of the first type and over the substrate in the areas of the transistors of the second type; and

- formation of a second silicon oxide layer in the areas of both types of peripheral transistors.

In accordance with a preferred embodiment, formation of the first and second silicon oxide layers takes place by means of a high-temperature treatment in an oxidizing ambient. The gate dielectric layer of all the peripheral transistors is therefore composed of an underlying silicon oxide layer formed by means of thermal treatment, having differentiated thickness, and an overlying silicon oxide layer deposited and densified by the above mentioned thermal treatment.

The gate dielectrics formed can be advantageously nitridized at the end of their formation if desired.

On the basis of the solution idea underlying the present invention the technical problem is solved by a process for the formation of an integrated circuit comprising non-volatile memory cells and peripheral transistors of the type described above and defined in the characterizing part of claims 1 and following.

The technical problem is also solved by an integrated circuit comprising non-volatile memory cells and peripheral MOS transistors of at least a first and a second types, in accordance with the description contained in the characterizing part of claims 10 and following.

The characteristics and advantages of the formation process in accordance with the present invention are set forth in the description of an embodiment thereof given below by way of non-limiting example with reference to the annexed drawings.

Brief description of the drawings

In the drawings:

FIGS. 1a-1e show diagrammatic cross section views of successive steps of a process for the formation of non-volatile memory cells and peripheral transistors of a first and a second type in accordance with the present invention.

Detailed description

The description of a formation process for memory cells and peripheral transistors in accordance with the present invention is given below with reference to a preferred embodiment as shown in FIGS. 1a-1e. These figures show unscaled diagrammatic cross section views and illustrate in succession the steps of a formation process for a non-volatile memory cell and at least a first and a second peripheral MOS transistors. The partial structures of the cell and the transistors are indicated respectively by reference numbers 1, 2 and 3. The regions R1, R2 and R3 represent the zones in

which are formed the cell 1 and the transistors 2 and 3.

The two transistors are distinguished from each other by the gate dielectric thickness, which is greater for the first transistor than for the second. In the memory circuit for example they represent respectively a high-voltage transistor and a low-voltage transistor.

There are shown in detail only the process steps more significant for the present invention as regards formation of the intermediate dielectric of the cell and the gate dielectric of the transistors.

The intermediate dielectric of the memory cell in accordance with the present invention consists as a whole of a triple layer comprising silicon oxide, silicon nitride and silicon oxide in succession.

The diagrammatic structure of the memory cell 1 is consistent with that of any non-volatile memory cell whether EPROM, EEPROM or FLASH, and consists of a floating gate MOS transistor. The peripheral transistors 2 and 3 are also MOS type in accordance with the present invention. The process to which reference is made specifically in the following description is a MOS type process, preferably performed with CMOS technology.

The initial steps of a process of formation of memory cells and peripheral transistors, not shown in the figures because conventional, comprise definition on a substrate 4 of semiconductor material, usually monocrystalline silicon, of insulation regions, where a thick silicon oxide layer, so-called field oxide, is formed and which delimit active area regions. It is noted that the cross sections shown in the figures are contained entirely in active area regions and therefore the field oxide is not visible.

Successively both in active area regions in which the memory cells will be formed and in external regions in which the peripheral transistors will be formed, and in particular in regions R1, R2 and R3, silicon oxide, indicated by 5 in the figures, is grown by means of high-temperature thermal oxidation of the substrate. The layer 5 represents the so-called gate oxide of the cells. The gate oxide layer of the cells is thin to allow transfer of the charge between the substrate and the floating gate by means of known physical mechanisms which depend on the type of non-volatile memory. Its thickness can vary indicatively between 70Å and 250Å, depending on the type of non-volatile memory cells and the programming and associated erasure mechanism.

Over this gate oxide layer 5 of the cells is formed a first layer of electroconductive material, indicated in FIG. 1a by 6 and which will constitute the floating gate of the cell 1. The layer 6 consists commonly of a first polycrystalline silicon layer, known briefly as poly 1, and is usually deposited over the entire silicon chip on which is integrated the circuit.

The process continues with conventional formation of the lower part of the intermediate dielectric layer of the memory cells. A silicon oxide layer 7 is formed alternatively by Chemical Vapor Deposition (CVD) or by means of high-temperature oxidation of the polysilicon

layer 6. In addition a silicon nitride layer 8 is deposited by the CVD technique.

Some steps which allow partial definition of the final structure of the cell, by means of removal in some zones of one or more layers from among those described above, are specific for each different non-volatile memory type. These are not described here for the sake of simplicity and are in any case conventional.

In accordance with the present invention, before formation of the upper part of the intermediate dielectric of the cells, the layers 7 and 8 of the intermediate dielectric, the polysilicon layer 6 and the gate oxide layer 5 of the cell 1 are removed in succession from the active peripheral areas, i.e. the regions R2 and R3 in which the peripheral transistors are to be formed. Removal takes place by means of a photolithographic technique of masking and successive chemical etching, at the end of which the mask of photosensitive material, usually a resin, is removed. FIG. 1a shows the structure of the memory cell 1 and the regions R2 and R3 assigned to the transistors 2 and 3 in this process step.

Advantageously removal of the mask used for the preceding etching can be followed by a step of cleaning the surface of the entire chip, preferably by means of acid etching, e.g. in hydrofluoric acid (HF). This step has the purpose of eliminating any possible residues of the mask which, being of organic material, introduces impurities, especially on the exposed surface of the substrate in the peripheral regions R2 and R3. The silicon nitride layer 8 of the intermediate dielectric is not damaged by an etching of the above mentioned type.

A silicon oxide layer, indicated in FIG. 1b by 9, is formed in this step of the process at least in the areas R2 and R3 of the peripheral transistors. Preferably this formation comprises an operation of oxidation in an oxidizing ambient at high-temperature. This layer 9 of silicon oxide is the so-called thermal type because achieved by means of a thermodynamic process of raising the temperature. The substrate is oxidized superficially in the active areas R2 and R3 of the transistors 2 and 3. On the other hand oxidation of the exposed surface of the silicon nitride layer 8 of the cell 1 due to this operation is negligible. The thermal oxide layer 9 will constitute part of the gate dielectric of the transistor 2.

The high-temperature oxidation treatment is preferably performed in an oxidizing ambient in an atmosphere containing oxygen (O_2) and/or steam (H_2O) and at a temperature between $750^\circ C$ and $950^\circ C$.

Then there is performed a step of masking the regions R1 and R2, of the cell 1 and the first transistor 2, to allow removal by means of a photolithographic technique and successive chemical etching of the silicon oxide layer 9 from the region R3 assigned to formation of the second transistor 3. FIG. 1c shows the three regions as they appear after removal of the mask.

In accordance with a preferred embodiment of the present invention the above mentioned removal of the layer 9 takes place if desired in two steps. First the silicon oxide layer 9 is partially removed from the region

R3. The mask used is then removed and the etching of the surface of the silicon oxide layer 9 is continued until complete removal of the layer so as to leave exposed the surface of the substrate in the region R3. This second etching step cleans the surface of the nitride layer 8 in the region R1 and the oxide layer 9 in the region R2 of the first transistor 2 of the possible contamination caused by the etching mask applied previously.

The intermediate dielectric of the cells is completed in the successive process step with formation by deposition of a silicon oxide layer 10, as shown in FIG. 1d. Deposition can take place by means of any of the chemical vapor deposition techniques and preferably by means of a High Temperature Oxidation (HTO) technique, i.e. any of the high-temperature CVD techniques. As chemical source there can be chosen one of the conventional ones, e.g. tetraethylorthosilicate, known to those skilled in the art as TEOS. The thickness of this deposited silicon oxide layer 10 is preferably between 50\AA and 250\AA . Its value depends on that of the underlying intermediate dielectric layers of the cell 1.

As shown in FIG. 1d the layer 10 is deposited not only in the region R1 of the matrix but also in the peripheral regions R2 and R3 where it will constitute the upper part of the gate dielectric of the first and second peripheral transistors 2 and 3.

Successively, to complete the gate dielectrics of the peripheral transistors, an additional silicon oxide layer is formed in the active areas both of the first transistor 2 and of the second transistor 3. The formation is performed in particular by means of an oxidation operation with a high-temperature treatment in oxidizing ambient to induce oxidation of the substrate surface. The thermal silicon oxide layer formed in this step is indicated by 11 in FIG. 1e. It represents the lower layer of the gate dielectric, which is in direct contact with the substrate because it is the result of oxidation of the substrate itself. It is noted that the line of demarcation between the layers 11 and 9 of the first transistor 2 is drawn symbolically with a broken line since the two layers at the end of their formation are essentially indistinguishable.

The oxidation operation for formation of the thermal silicon oxide layer 11 permits advantageously the simultaneous densification of the overlying deposited silicon oxide layer 10.

Preferably growth of the additional silicon oxide layer 12 takes place by using parameters similar to those chosen above for formation of the silicon oxide layer 10. Therefore this step is performed preferably in an oxidizing ambient at a temperature between $750^\circ C$ and $950^\circ C$ and in an atmosphere containing at least one of the following gasses: oxygen (O_2) and steam (H_2O).

The thicknesses values of the gate dielectrics of the first and second transistors, preset on the basis of the specific application, are achieved in this step.

Formation of the intermediate dielectric multilayer of the cell 1 and the gate dielectric of the peripheral transistors 2 and 3 in accordance with the present

invention is completed if desired by a nitridizing process performed by means of annealing in an ambient containing N_2O , to further increase the quality and reliability of the gate dielectrics.

The gate dielectric of both the peripheral transistors 2 and 3 therefore comprises, in the preferred embodiment of the present invention, a double layer. Specifically a thermal silicon oxide layer, 11+9 or 11 respectively for the first and second transistors, is in direct contact with the substrate and a deposited silicon oxide layer is overlying. The latter appears in both the transistors as an extension of the upper silicon oxide layer of the intermediate dielectric multilayer of the cell 1.

In accordance with the present invention the overall thicknesses of the gate oxides of both types of transistor are indicatively between 70Å and 350Å. The thermal oxide thicknesses also fall within this range.

After the above described formation of the intermediate dielectric multilayer of the cell and the gate dielectric of the peripheral transistors, completion of the cell and the transistors takes place through standard process steps. In particular a second polysilicon layer, or poly 2, and if desired a silicide layer are deposited and then patterned for the simultaneous formation of the control gate of the cell and of the gate of the transistors. The process is completed by appropriate implantations, formation of a passivation layer and of the interconnections by means of opening of contacts, and deposition of one or more metallization layers.

Therefore in the process in accordance with the present invention the gate dielectric of the transistors is not formed at the end of formation of the intermediate dielectric of the cells. Deposition of the last silicon oxide layer of the intermediate dielectric allows to achieve simultaneously also the gate dielectric upper layer. Advantageously in accordance with the present invention, in the transistors 2 and 3 the final thermal oxide layer 11 is formed after the overlying deposited oxide layer 10. This permits formation of the thermal oxide layer and simultaneous densification, as mentioned above, of the layer 10 without further steps such as thermodynamic annealing processes which are essential in accordance with the prior art for curing the deposited layer and to ensure operation of the device.

The proposed solution, in which the deposited silicon oxide layer is then densified in at least one successive oxidation step, thus provides gate dielectrics with better quality both in terms of defects and in terms of electrical qualities.

The use of a double layer for formation of gate dielectrics whose upper part is deposited prevents formation of defects in the gate dielectric if considered as a whole. Indeed, a defect in one of the layers is covered by the other and the simultaneous presence of two defects at exactly the same point in the layer is highly improbable.

Furthermore the upper layer being deposited is conformal to the underlying structures, so allowing to

cover irregular growths of oxides in critical positions, e.g. of the field oxide layer at its edges.

It should be remembered that the thermal oxide and the oxide deposited in accordance with the present invention are distinguishable by means of electrical, physical and optical measurements because they have different dielectric constants.

It is noted that the process in accordance with the present invention has the advantage of allowing formation of distinct layers of silicon oxide whose thicknesses can be chosen independently. The only fixed value for formation of the layers making up the gate dielectric of the transistors is that of the deposited oxide layer, whose thickness should be determined, as known to those skilled in the art and as mentioned above, on the basis of the relative thickness of the other two layers contained in the intermediate dielectric to ensure good operation thereof.

The process in accordance with the present invention is particularly simple and its embodiment does not present manufacturing difficulties.

Another advantage of the described process is the flexibility in particular in the use of optional cleaning steps, described above in the explanation of the individual process steps, for optimization of the functionality of the dielectrics.

Of course to the process for the embodiment of non-volatile memory cells and peripheral transistors in accordance with the present invention described above can be made modifications and variations all however falling within the scope of the present invention as defined in the following claims.

Claims

1. Process for forming an integrated circuit in a monocrystalline silicon substrate (4) of the type in which is provided for the implementation of at least one matrix of non-volatile memory cells (1) in each of which a floating gate and a control gate, both electroconductive, are insulated electrically from each other by means of an intermediate dielectric multilayer comprising a lower silicon oxide layer (7), an intermediate silicon nitride layer (8) and an upper silicon oxide layer (10) and the simultaneous implementation in peripheral zones of the memory cells of at least a first (2) and a second (3) transistors type having gate dielectric of a first and a second thickness respectively, characterized in that, after formation of the floating gate with a gate oxide layer (5) and a polycrystalline silicon layer (6) and the formation of the lower silicon oxide layer (7) and the intermediate silicon nitride layer (8), it comprises the step of:

- removal of the above mentioned layers from the zones (R2,R3) peripheral to the matrix;
- formation of a first silicon oxide layer (9) over

- the substrate in the areas (R2,R3) of both transistor types (2,3);
- removal of the previous layer (9) from areas (R3) assigned only to the transistors (3) of the second type;
 - deposition of said upper silicon oxide layer (10) over the memory cells (1), over the first silicon oxide layer (9) in the areas (R2) of the transistors (2) of the first type and over the substrate (4) in the areas (R3) of the transistors of the second type; and
 - formation of a second silicon oxide layer (11) in the areas (R2,R3) of both types of peripheral transistors (2,3).
2. Process in accordance with claim 1 and characterized in that the formation step of said second silicon oxide layer (11) comprises a high-temperature treatment in an oxidizing ambient.
 3. Process in accordance with claim 2 and characterized in that said high-temperature treatment is performed in an oxidizing ambient at a temperature between 750°C and 950°C in an atmosphere containing at least one of the following compounds O₂ and H₂O.
 4. Process in accordance with claim 1 and characterized in that formation of said first silicon oxide layer (9) comprises a step of high-temperature oxidation.
 5. Process in accordance with claim 4 and characterized in that said oxidation operation is performed in an oxidizing ambient at a temperature between 750°C and 950°C in an atmosphere containing at least one of the following compounds O₂ and H₂O.
 6. Process in accordance with claim 1 and characterized in that it comprises a step of high-temperature nitridizing of the second silicon oxide layer.
 7. Process in accordance with claim 1 and characterized in that removal of the first silicon oxide layer (9) from areas (R3) of the transistors (3) of the second type comprises a first step of partial removal of said layer (9) in said areas (R3) and a successive removal step on portions of the silicon chip at least including regions (R1,R2) not subjected to the first removal step up to completion in the above mentioned areas (R3) of removal of the first silicon oxide layer (9).
 8. Process in accordance with claim 1 and characterized in that it is implemented with CMOS technology.
 9. Process in accordance with claim 1 and characterized in that the thickness of said upper deposited silicon oxide layer (10) is between 50Å and 250Å and that said first and said second thicknesses of the gate dielectric (9-11;10-11) are between 70Å and 350Å.
 10. Integrated circuit on a monocrystalline substrate of the type comprising at least matrix of one non-volatile memory cells (1) in each of which a floating gate and a control gate, both electroconductive, are insulated electrically from each other by means of an intermediate dielectric multilayer including at least one upper silicon oxide layer (10) and comprising additionally in zones peripheral (R2,R3) to the matrix at least one first (2) and one second (3) transistor type having gate dielectric of a first and a second thickness respectively; and characterized in that the multilayer gate dielectric of both types of peripheral transistors includes an underlying silicon oxide layer (9,11;11) formed by means of thermal treatment and an overlying deposited silicon oxide layer (10) densified by said thermal treatment.
 11. Integrated circuit in accordance with claim 10 and characterized in that said deposited silicon oxide layer (10) of the gate dielectrics constitutes the extension of the upper silicon oxide layer of the intermediate dielectric multilayer.
 12. Integrated circuit in accordance with claim 10, in which said transistors of the first and second types (2,3) are high voltage and low voltage transistors respectively and characterized in that said second thickness of the gate dielectric (10,11) of the second transistor type (3) is less than said first thickness of the corresponding layer (9-11) of the first transistor type (2).
 13. Integrated circuit in accordance with claim 10 and characterized in that the thickness of the thermal silicon oxide layer (11) of said second transistor type (3) is less than that of (9,11) of said first transistor type (2).
 14. Integrated circuit in accordance with claim 10 and characterized in that at least one of said multilayer gate dielectrics is nitridized.
 15. Integrated circuit in accordance with claim 10 and characterized in that the thickness of said deposited silicon oxide layer (10) is between 50Å and 250Å and said first and second thickness of the gate dielectric (9-11; 10-11) are between 70Å and 350Å.



Fig. 1a

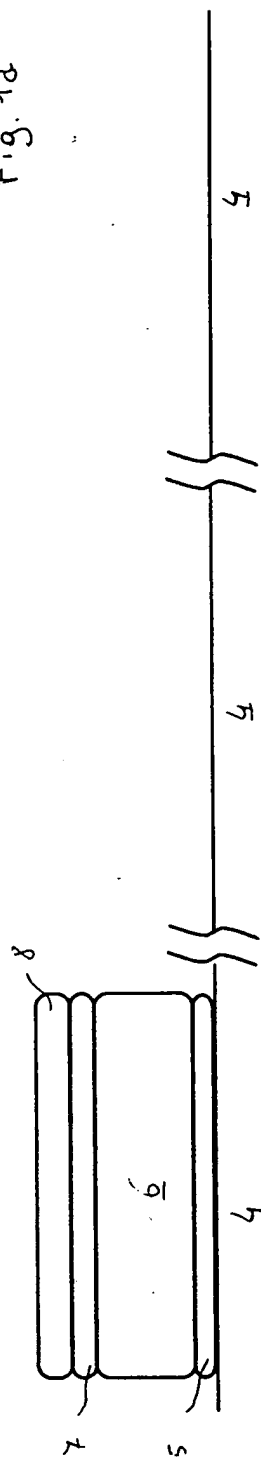
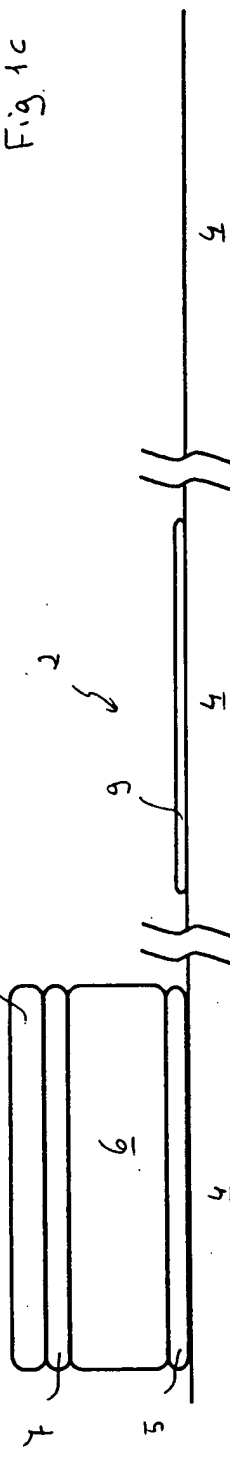


Fig. 1b



Fig. 1c



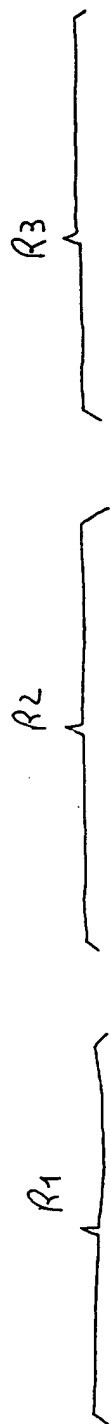


Fig. 1d

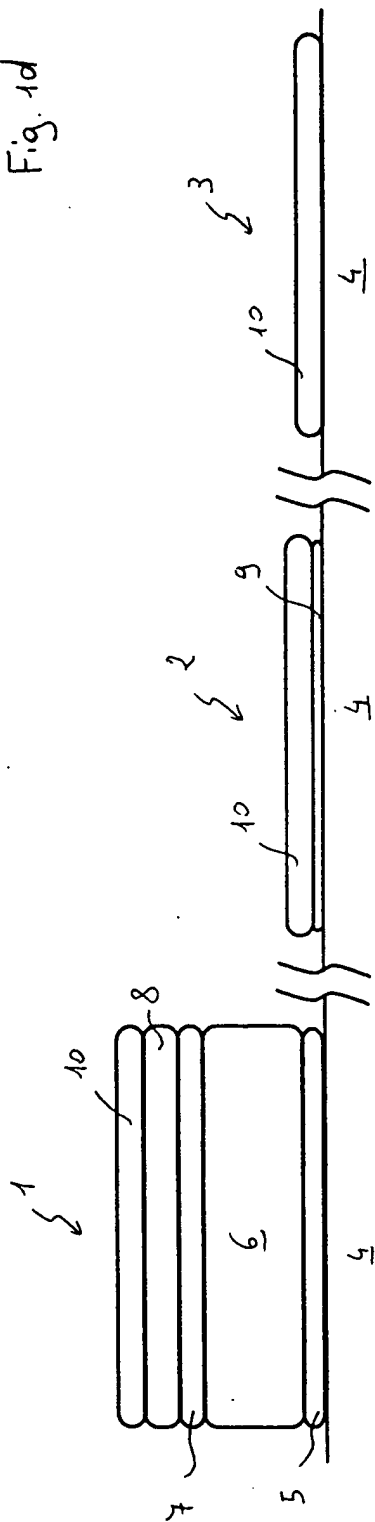
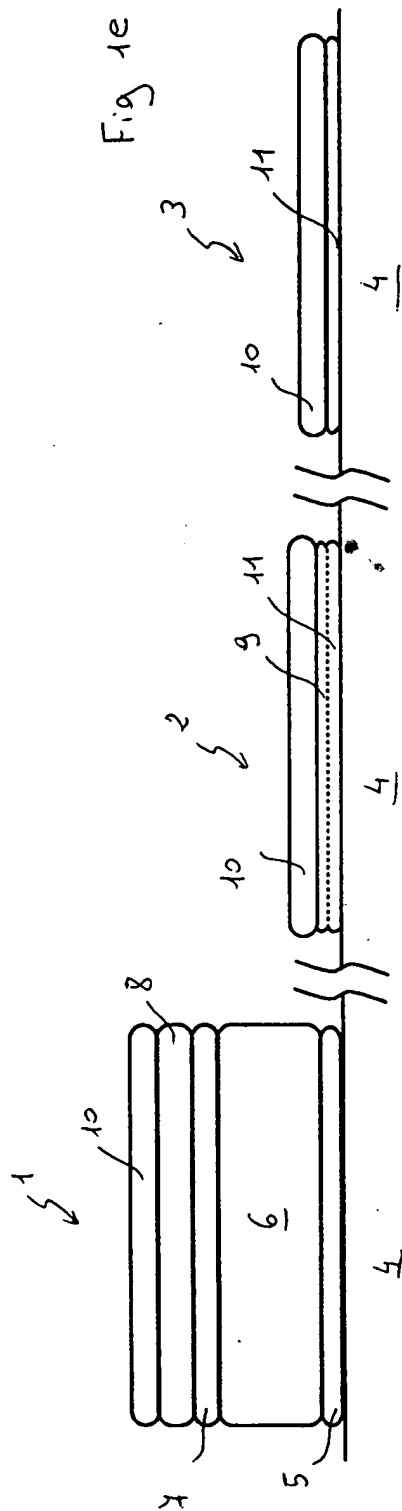


Fig. 1e





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 83 0282

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	US-A-4 471 373 (SHIMIZU ET AL.) * the whole document *	10-14	H01L21/8247 H01L27/115
D,Y	IEEE IEDM TECHNICAL DIGEST 93, 1993 pages 321-324, XP 000481625 HSING-HUANG TSENG ET AL. 'THIN CVD STACKED GATE DIELECTRIC FOR ULSI TECHNOLOGY'	10-14	
A	* the whole document *	1-9,15	
Y	US-A-4 780 424 (HOLLER ET AL.) * column 5, line 9 - line 15 *	14	
D,A	US-A-5 104 819 (FREIBERGER ET AL.) * the whole document *	1-15	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H01L
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 29 November 1995	Examiner Onshage, A
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